What is claimed is:

1. A device comprising:

a supply node for providing a supply source;

a memory array having multiple memory segments, each connected to the supply node via a supply path for receiving the supply source;

a supply control circuit connected in the supply path for isolating a selected memory segment of the multiple memory segments from the supply node if the selected memory segment is defective; and

a redundant array for replacing the selected memory segment if the selected memory segment is defective.

2. The device of claim 1, wherein the multiple memory segments connect in parallel with each other, and wherein each memory segment of the multiple memory segments connects in series with the supply control circuits and the supply node.

3. The device of claim 2, wherein the supply control circuit includes a plurality of switching units, each of the switching units connecting in series with one memory segment of the multiple memory segments and the supply node.

4. The device of claim 1, wherein each memory segment of the multiple memory segments includes a memory cell having more than two transistors.

5. A device comprising:

a first supply node and a second supply node;

a supply control circuit connected between the first supply node and a plurality of internal nodes;

a plurality of memory segments, each of the memory segments connecting between one of the internal nodes and the second supply node; and

at least one redundant segment connected to the memory segments for maintaining a storage capacity of device when at least one of the memory segments is defective.

6. The device of claim 5, wherein at least one of the memory segments is defective.

7. The device of claim 5, wherein at least one of the memory segments has a circuit short between one of the internal nodes and the second supply node.

8. The device of claim 5, wherein the supply control circuit includes a plurality of switching units, each of the switching units connecting between the first supply node and one of the internal nodes.

9. The device of claim 8, wherein one of the switching units includes a transistor having a source and a drain connected between the first supply node and one of the internal nodes.

10. The device of claim 5, wherein each of the memory segments includes a plurality of memory cells, each of the memory cells connecting between one of the internal nodes and the second supply node.

11. The device of claim 10, wherein at least one of the memory segments has a defective memory cell.

12. The device of claim 10, wherein at least one of the memory segments has a circuit short in one of the memory cells between one of the internal nodes and the second supply node.

13. A device comprising:

a first supply node and a second supply node;

a plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes;

a plurality of switching units, each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes, wherein each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal; and

a redundant array for replacing at least one memory segment of the plurality of memory segments.

14. The device of claim 13 further comprising a redundancy controller connected to the switching units for selectively setting the state of the select signal based on a number of programming signals.

15. The device of claim 14 further comprising a programming unit for generating the programming signals based on a programmed address stored in the programming unit.

16. The device of claim 13, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective.

17. A device comprising:

a plurality of supply paths connected to a supply node;

a plurality of memory segments, each of the memory segments connecting to the supply node via one of the supply paths;

a plurality of switching units, each of the switching units connecting in one of the supply paths and connecting to a corresponding memory segment, the corresponding memory segment being one of the memory segments; wherein each of the switching units includes an enable mode for connecting the corresponding

memory segment to the supply node, and a disable mode for disconnecting the corresponding memory segment from the supply node; and

at least one redundant segment for replacing at least one memory segment of the plurality of memory segments.

18. The device of claim 17, wherein at least one of the memory segments is defective.

19. The device of claim 17, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory cell groups of at least one of the memory segments is defective.

20. The device of claim 17, wherein each of the switching units includes a transistor for switching one of the switching units between the enable and disable modes.

21. The device of claim 17, wherein each of the switching units includes an input node for receiving a select signal to switch a corresponding switching unit to the disable mode if the corresponding memory segment is defective, the corresponding switching unit being one of the switching units.

22. The device of claim 17, wherein each of the switching unit includes a control input node for receiving a select signal to switch the corresponding switching unit to the enable mode if the corresponding memory segment is non-defective, the corresponding switching unit being one of the switching units.

23. A device comprising:

a first supply node and a second supply node;

a plurality of switching units, each of the switching units connecting to the first supply node; and

a plurality of memory segments, each of the memory segments connecting to the first supply node through one of the switching units and including a resistance between an internal node and the second supply node, wherein the internal node connecting to one memory segment is different from the internal node connecting to another memory segment, wherein the resistance of at least one memory segment equals a first resistance.

24. The device of claim 23, wherein the memory segment having the first resistance is defective.

25. The device of claim 23, wherein each of the memory segments includes equal number of memory cells.

26. The device of claim 25, wherein the resistance of at least one of the memory segments equals a second resistance, wherein the first resistance and the second resistance are unequal.

27. The device of claim 23, wherein the memory segment having the first resistance has a circuit short between the second supply node and the internal node connected to the memory segment having the first resistance.

28. The device of claim 23, wherein one of the switching unit includes a transistor connected between the first supply node and one of the memory segments.

29. A device comprising:

a memory cell including a first storage node and a second storage node and including:

a latch connected to the first and second storage nodes and to an internal node;

a first access element for accessing the first storage node; and

a second access element for accessing the second storage node; and

a switching unit connected between the internal node and a supply node.

30. The device of claim 29, wherein the switching unit includes a transistor having a source and a drain connected between the internal node and the supply node.

31. The device of claim 29, wherein the latch includes:

a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and

a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

32. The device of claim 31, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

33. The device of claim 29, wherein the latch includes:

a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and

a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

34. A device comprising:

a plurality of memory cells, at least one of the memory cells connecting between a first internal node and a second internal node and including:

a first storage node and a second storage node;

a latch connected to the first and second storage nodes and connected between the first and second internal nodes;

a first access element for accessing the first storage node; and

a second access element for accessing the second storage node;

a first switching unit connected between the first internal node and a first supply node; and

a second switching unit connected between the second internal node and a second supply node.

35. The device of claim 34, wherein the latch includes:

a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and

a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

36. The device of claim 35, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

37. The device of claim 34, wherein the first switching unit includes a transistor having a source and a drain connected between the first internal node and the first supply node.

38. The device of claim 37, wherein the second switching unit includes a transistor having a source and a drain connected between the second internal node and the second supply node.

39. The device of claim 34, wherein the latch includes:

a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and

a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

40. A device comprising:

a first supply node and a second supply node;

a plurality of memory segments, each of the memory segments connecting between the first supply node and an internal node, each of the memory segments including a plurality of memory cells, each of the memory cells including:

a first storage node and a second storage node;

a latch connected to the first and second storage node and connected in between the first supply node and the internal node;

a first access element for accessing the first storage node; and

a second access element for accessing the second storage node; and

a plurality of switching units, each of the switching units connecting between one of the memory segments and the second supply node.

41. The device of claim 40, wherein at least one of the memory segments is defective.

42. The device of claim 40, wherein at least one of the memory segments has a circuit short between the first supply node and the internal node.

43. The device of claim 40, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory cell groups of at least one of the memory segments is defective.

44 The device of claim 40, wherein the switching unit includes a transistor having a source and a drain connected between the internal node and the supply node.

45 The device of claim 40 wherein the latch includes:

a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and

a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

46. The device of claim 45 wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

47. The device of claim 40, wherein the latch includes:

a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and

a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

48. A device comprising:

a first supply node and a second supply node;

a plurality of memory segments, each of the memory segments including a plurality of memory cells, each of the memory cells including:

a first storage node and a second storage node;

a latch connected to the first and second storage node and connected in between a first internal node and a second internal node;

a first access element for accessing the first storage node; and

a second access element for accessing the second storage node;

a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments; and

a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments.

49. The device of claim 48, wherein at least one of the memory segments is defective.

50. The device of claim 48, wherein at least one of the memory segments has a circuit short between the first and second internal nodes

51. The device of claim 48, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective.

52. The device of claim 48, wherein in each of the memory segments, the plurality of memory cells are arranged in a plurality of rows connected in parallel between one of the first switching unit and one of the second switching units.

53. The device of claim 48, wherein each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments.

54. The device of claim 48, wherein each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments.

55. The device of claim 48, wherein the latch includes:

a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and

a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

56. The device of claim 55, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

57. The device of claim 48, wherein the latch includes:

a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and

a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

58. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a supply node for providing a voltage source;

a memory array connected to the supply node via a supply path for receiving the voltage source;

a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective; and

a redundant array for replacing the memory segment if the memory segment is defective.

59. The system of claim 58, wherein memory array includes a plurality of memory segments connected in parallel with each other, each of the memory segments connecting in series with the supply control circuits and the supply node.

60. The system of claim 59, wherein at least one of the memory segments is defective.

61. The system of claim 59, wherein the supply control circuit includes a plurality of switching units, each of the switching units connecting in series with one of the memory segments and the supply node.

62. The system of claim 58 further comprising a redundant array for replacing the memory segment if the memory segment is defective.

63. A method comprising:

determining a condition of a memory device;

isolating a memory segment of the memory device from a supply source if the memory segment is defective; and

replacing the memory segment with a redundant segment if the memory segment is defective.

64. The method of claim 63, wherein determining a condition of a memory device includes detecting for a defect in a memory array of the memory device.

65. The method of claim 63, wherein isolating the memory segment includes electrically disconnecting the memory segment from the supply source.

66. A method comprising:

determining a condition of a plurality of memory segments;

storing an address of a selected memory segment among the memory segments if the selected memory segment is defective;

isolating the selected memory segment from a supply source if the selected memory segment is defective; and

replacing the selected memory segment with a redundant segment if the selected memory segment is defective.

67. The method of claim 66, wherein determining a condition of a memory device includes detecting for a defect of at least one of the memory segments.

68. The method of claim 67, wherein detecting for a defect includes detecting for a circuit short between a supply node and an internal node connecting to one of the memory segments.

69. The method of claim 66, wherein storing includes programming a number of programmable elements.

70. The method of claim 66, wherein isolating the selected memory segment includes electrically disconnecting the selected memory segment from the supply source.

71. A method comprising:

testing a plurality of memory segments in which at least one of the memory segments at an unknown address is defective;

identifying an address of a defective memory segment of the plurality of memory segments;

storing the address as stored address;

isolating the defective memory segment from a voltage source based on the stored address; and

replacing the defective memory segment with a redundant segment based on the stored address.

72. The method of claim 71, wherein testing includes writing and reading data to and from the memory segments.

73. The method of claim 71, wherein identifying an address includes comparing a result of a test with a known result.

74. The method of claim 71, wherein storing includes programming a plurality of programming elements.

75. The method of claim 71, wherein isolating the defective memory segment includes electrically disconnecting the defective memory segment from the voltage source.